What is claimed is:

1. A high-voltage detecting circuit comprising:

an input terminal which is commonly applied with a high voltage and an input signal, said high voltage being higher than a power supply voltage and said input signal having a voltage equal to or lower than the power supply voltage;

a reset unit for outputting an initial reset signal when the power supply is turned on;

a transistor having a source connected to said input terminal and a gate applied with the power supply voltage, said transistor turning on in response to the application of said high voltage to said input terminal, and turning off in response to the application of the input signal to said input terminal; and

a latch which is reset by the initial reset signal, and set when said transistor is turned on to output a high-voltage detecting signal.

2. A high-voltage detecting circuit comprising:

an input terminal which is commonly applied with a high voltage and an input signal, said high voltage being higher than a power supply voltage and said input signal having a voltage equal to or lower than the power supply voltage;

a reset unit for outputting an initial reset signal when the power supply is turned on;

a first transistor having a source and a drain connected to said input terminal and a first node, respectively, and a gate applied with the power supply voltage, said first transistor turning on in response to the application of said high voltage

to said input terminal, and turning off in response to the application of the input signal to said input terminal;

a pull-down device connected between said first node and a ground potential;

an inverter for inverting a logical value at said first node;

a second transistor connected between the power supply voltage and a second node, said second transistor being controlled between on state and off state by an output signal from said inverter;

a third transistor connected between said second node and the ground potential, which turns on in response to the initial reset signal applied thereto; and

a latch for holding a potential at said second node to output the potential as a high-voltage detecting signal.

3. A high-voltage detecting circuit according to claim 2, further comprising:

a fourth transistor connected between said second node and the ground potential, which turns on in response to a mode reset signal applied thereto.

4. A high-voltage detecting circuit comprising:

an input terminal which is commonly applied with a high voltage and an input signal, said high voltage being higher than a power supply voltage and said input signal having a voltage equal to or lower than the power supply voltage;

a first transistor having a source and a drain connected to said input terminal and a first node, respectively, and a gate applied with the power supply voltage, said first transistor

turning on in response to the application of said high voltage to said input terminal, and turning off in response to the application of the input signal to said input terminal;

a first pull-down device connected between said first node and a ground potential;

an inverter for inverting a logical value at said first node;

a second transistor connected between the power supply voltage and a second node, said second transistor being controlled between on state and off state by an output signal from said inverter;

a second pull-down device connected between said second node and the ground potential;

a third transistor connected between said second node and the ground potential, which turns on in response to an external reset signal applied thereto; and

a latch for holding a potential at said second node to output the potential as a high-voltage detecting signal.

5. A high-voltage detecting circuit according to claim 1, further comprising an internal circuit connected to said input terminal, wherein said high voltage is applied to said input terminal for setting a mode for said internal circuit.

6. A high-voltage detecting circuit according to claim 5, wherein said mode is set when said internal circuit is tested.

7. A high-voltage detecting circuit according to claim 1, wherein said latch includes two inverters comprised of flip-flops.

8. A high-voltage detecting circuit according to claim 2,

wherein said pull-down device includes a depletion type MOS transistor.

9. A high-voltage detecting circuit according to claim 4, wherein said pull-down device includes a depletion type MOS transistor.

10. A high-voltage detecting circuit according to claim 2, further comprising an internal circuit connected to said input terminal, wherein said high voltage is applied to said input terminal for setting a mode for said internal circuit.

11. A high-voltage detecting circuit according to claim 3, further comprising an internal circuit connected to said input terminal, wherein said high voltage is applied to said input terminal for setting a mode for said internal circuit.

12. A high-voltage detecting circuit according to claim 4, further comprising an internal circuit connected to said input terminal, wherein said high voltage is applied to said input terminal for setting a mode for said internal circuit.

13. A high-voltage detecting circuit according to claim 2, wherein said latch includes two inverters comprised of flip-flops.

14. A high-voltage detecting circuit according to claim 4, wherein said latch includes two inverters comprised of flip-flops.